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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,884	07/12/2001	Ronald J. Melanson	03226/053002;P5039	3596

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EXAMINER	
CHASE, SHELLY A	

ART UNIT	PAPER NUMBER
2133	6

DATE MAILED: 12/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/904,884	Applicant(s) MELANSON ET AL.	
	Examiner Shelly A Chase	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1 to 16 are presented for examination.

Information Disclosure Statement

2. The references listed in the information disclosure statement submitted on 6-19-2002 have been considered by examiner (see attached PTO-1449).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims **1** to **4, 6** to **10**, and **12** to **16** are rejected under 35 U.S.C. 102(b) as being anticipated by Lordi (USP 5611042).

Claim **1**:

Lordi discloses a memory unit being corrected via error detection and error correction through a micro-controller (see fig. 2), the system comprising; a static random access memory (SRAM 1) and a second memory (SRAM2) (see col. 2, lines 40 to 45), and a parity selection logic [50] for receiving data from SRAM1 and SRAM2 (see col. 2, lines 50 to 52). Lordi also teaches that a multiplexer [40] is connected to SRAM1 and SRAM2 via data lines [32 & 34] and the mulitplexer selects data from SRAM2 if the

parity select logic detects an error in the read data (see col. 2, lines 65 et seq.), which reads on "wherein input selection of the multiplexer is controlled by an output of the error checking circuit."

As per claims **2** and **3**, Lordi teaches the memories are SRAM (see col. 2, lines 33 to 35) and a parity checking device for detecting errors (see col. 2, lines 50 to 51).

As per claim **4**, Lordi discloses the parity select logic selects data from the primary memory if no errors are found and select data from the backup memory if an error is detected on the data read (see col. 2, lines 60 et seq.).

As per claim **6**, Lordi discloses simultaneous read and write operations for the memory devices (see col. 4, lines 1 to 12).

Claims **7** and **16**:

Lordi discloses a memory unit being corrected via error detection and error correction through a micro-controller (see fig. 2), comprising; a static random access memory (SRAM 1) and a second memory (SRAM2) (see col. 2, lines 40 to 45), and a parity selection logic [50] ("means for error checking") for receiving data from SRAM1 and SRAM2 and parity checking the data for errors outputting a signal to select data from either the primary memory or the backup memory(see col. 2, lines 50 to 52). Lordi also teaches a simultaneous read and write process to the memories (see col. 4, lines 18 to 11), and that a multiplexer [40] is connected to SRAM1 and SRAM2 via data lines [32 & 34] wherein the mulitplexer selects data from SRAM2 if the parity select logic detects an error in the read data (see col. 2, lines 65 et seq.).

As per claims **8** to **10**, Lordi discloses the memory devices are static random access memories (SRAM1 and SRAM2), a parity select logic [50] detecting and correcting errors and a multiplexer for selecting data from the primary memory or the backup memory.

Claim **12**:

Lordi discloses a method for error correction and detection for a memory unit, the method comprising: a simultaneous read and write operation to (SARM1 and SARM 2), (see col. 4, lines 1 to 13), a RAM select logic selects the address for data to be read from the first or second SRAM (see col. 3, lines 35 to 42), and a parity select logic [50] checking the data read from specified locations of both SRAm1 and SRAM2 for errors and outputting a signal to select data based on the detection of errors (see col. 2, lines 40 et seq.).

As per claims **13** to **15**, Lordi discloses parity select logic for detecting errors, a multiplexer [40] selecting data and data and parity stored in the memory are read by a byte (see fig. 5).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **5** and **11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lordi in view of Plants (USP 6237124 B1).

As per claims **5** and **11**, Lordi does not clearly teach that the first and second memory, the error checking means and the selection means are implemented on a single chip. However, Plants in an analogous art teaches a method for error checking in the configuration SRAM of a field programmable array (FPGA) wherein the configuration SRAM, a user SRAM a CRC circuit and a multiplexor are implemented in a FPGA (see col. 4, lines 15 to 25).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify checking errors in the memory unit of Lordi to include all the elements on a single chip as taught by Plants since, Plants discloses utilizing a single chip aids in better performance and flexibility. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to employ a method to achieve better performance when checking a memory unit for errors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A Chase whose telephone number is 703-308-7246. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Shelly A Chase